IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Chen et al.

Serial No.: 09/748,256 Group Art Unit: 2811

Filed: December 27, 2000 Examiner: Ori Nadav

For: METHOD FOR FABRICATING COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) DEVICES ON A MIXED BULK AND SILICON-ON-INSULATOR (SOI) SUBSTRATE

6/B
FJONES
7-9-01

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action dated March 29, 2001, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please replace the title as follows: - - SEMICONDUCTOR DEVICE ON A COMBINATION BULK SILICON AND SILICON-ON-INSULATOR (SOI) SUBSTRATE

IN THE CLAIMS:

Please cancel claims 24-28 without prejudice or disclaimer.

Please add the following new claims:

B1 Sub C1

- - 29. A semiconductor device comprising:

a bulk silicon region; and

a silicon-on-insulator (SOI) region comprising:

a crystallized silicon layer formed by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions, and

isolation oxides formed in said isolation trenches.

Sub D2

30. The semiconductor device according to claim 29, wherein islands of crystallized